

Application No.: 10/033,748

Docket No.: JCLA7648

In The Claims:

1. (currently amended) A MOSFET structure comprising:
a substrate;
a tortuous gate line on the substrate;
a gate dielectric layer between the tortuous gate line and the substrate; and
a source region and a drain region in the substrate beside the tortuous gate line, wherein
along a longitudinal axis of the tortuous gate line, the source region has-a is broader-part beside a
first segment of the gate line and is a-narrower beside a second segment of the gate line-part, and
along the longitudinal axis of the tortuous gate line, the drain region has-a-is broader beside a
second segment part of the gate line and is a-narrower beside a first segment of the gate line-part,
wherein the-a broader part-of-the source region is disposed opposite to the-a narrower part-of-the
drain region and the-a narrower part-of-the source region is disposed opposite to the-a broader
part-of-the drain region.

2. (currently amended) The MOSFET structure of claim 1, wherein at least a contact is
disposed on the broader ~~part-of-the~~ source region and at least a contact is disposed on a-the
~~broader-part-of-the~~ drain region.

3. (original) The MOSFET structure of claim 1, wherein the material of the tortuous gate
line comprises doped polysilicon.

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4. (currently amended) A MOSFET structure comprising:

a substrate;

a tortuous gate line on the substrate;

a gate dielectric layer between the tortuous gate and the substrate;

a source region and a drain region disposed within the substrate adjacent to the tortuous gate, wherein along a longitudinal axis of the tortuous gate line, the source region has a is broader beside a first segment of the gate line part and a is narrower beside a second segment of the gate line part, and the drain region has a is broader beside a second segment of the gate line part and is a narrower beside the first segment of the gate line part, wherein the a broader part of the source region is disposed opposite to the a narrower part of the drain region, and the a narrower part of the source region is disposed opposite to the a broader part of the drain region; and

a metal-silicide layer disposed on the tortuous gate and on the source and drain regions.

5. (currently amended) The MOSFET structure of claim 4, wherein at least a contact is disposed on the broader ~~part of the~~ source region and at least a contact is disposed on a the broader part of the drain region.

6. (original) The MOSFET structure of claim 4, wherein the material of the tortuous gate line comprises doped polysilicon.

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7. (original) The MOSFET structure of claim 4, wherein the material of the metal-silicide layer is selected from the group comprising titanium silicide, cobalt silicide, nickel silicide, and palladium silicide.

8. (currently amended) A metal oxide semiconductor device comprising:

a substrate;

a tortuous gate on the substrate;

a gate dielectric layer between the tortuous gate and the substrate;

a lightly doped source region, a source region, a lightly doped drain region, and a drain region disposed within the substrate located adjacent to the tortuous gate line, wherein along a longitudinal axis of the tortuous gate line, the lightly doped source region, the source region beside one segment of the tortuous gate line are broader, and the lightly doped drain region, and the drain region are narrower beside the one segment of the tortuous gate line have a broader part and a narrower part, respectively, while along the longitudinal axis of the tortuous gate line, the lightly doped source region, the source region are narrower beside another segment of the tortuous gate line, the lightly doped drain region, and the drain region are broader beside the another segment of the tortuous gate line, wherein the a broader part of the lightly doped source region / source region is opposite to the a narrower part of the lightly doped drain region / drain region, and the a narrower part of the lightly doped source region / source region is opposite to the a broader part of the lightly doped drain region / drain region; and

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a first metal silicide layer disposed on the tortuous gate and a second metal silicide layer disposed on the source and drain regions.

9. (currently amended) The metal oxide semiconductor device of claim 8, wherein at least a contact is disposed on the broader ~~part of the~~ source region and at least a contact is disposed on ~~at the~~ broader ~~part of the~~ drain region.

10. (original) The metal oxide semiconductor device of claim 8, wherein the material of the gate comprises doped polysilicon.

11. (original) The metal oxide semiconductor device of claim 8, wherein the material of the first metal-silicide layer is selected from one of the group comprising titanium silicide, cobalt silicide, nickel silicide, and palladium silicide.

12. (original) The metal oxide semiconductor device of claim 8, wherein the material of the second metal-silicide layer is selected from one of the group comprising titanium silicide, cobalt silicide, nickel silicide, and palladium silicide.

13. (original) The metal oxide semiconductor device of claim 8, wherein the material of the first metal-silicide layer on the tortuous gate and the material of the second metal silicide layer of the source/drain regions are substantially of same material.

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14. (original) The metal oxide semiconductor device of claim 8, wherein the material of the first metal-silicide layer on the tortuous gate is different from that of the second metal-silicide layer on the source/drain region.

15. (original) The metal oxide semiconductor device of claim 8, wherein the material of the first metal-silicide layer is titanium silicide.

16. (original) The metal oxide semiconductor device of claim 8, wherein the material of the second metal-silicide layer on the source/drain region is titanium silicide.

17. (currently amended) A metal oxide semiconductor device comprising:
a tortuous gate line on the substrate;
a gate dielectric layer between the tortuous gate line and the substrate; and
a lightly doped source region, a source region, a lightly doped drain region, and a drain region disposed within the substrate located adjacent to the tortuous gate line, wherein along a longitudinal axis of the tortuous gate line, the lightly doped source region, the source region beside one segment of the tortuous gate line are broader, and the lightly doped drain region, and the drain region are narrower beside the one segment of the tortuous gate line have a broader part and a narrower part, respectively, while along the longitudinal axis of the tortuous gate line, the lightly doped source region, the source region are narrower beside another segment of the tortuous gate line, and the lightly doped drain region, the drain region are broader beside the

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another segment of the tortuous gate line, wherein ~~the~~ a narrower part of the lightly doped source region / source region is opposite to ~~the~~ a broader part of the lightly doped drain region / drain region, and ~~the~~ a broader part of the lightly doped source region / source region is opposed to ~~the~~ a narrower part of the lightly doped drain region / drain region.

18. (currently amended) The metal oxide semiconductor device of claim 17, wherein at least a contact is disposed on the broader ~~part of the~~ source region and at least a contact is disposed on ~~a~~ the broader ~~part of the~~ drain region.

19. (original) The metal oxide semiconductor device of claim 17, wherein the material of the gate line comprises doped polysilicon.